REMARKS

The Final Office Action mailed on December 15, 2006 has been reviewed, along with the art cited. Claims 1-6, 19-20, 28-32, 35-41, and 43-56 are pending in this application. Claim 45 has been amended and claims 9-17 and 21-26 have been cancelled. Claims 57-59 have been added.

Rejections Under 35 U.S.C. § 103

Claims 1-6, 28-32, 35-39, 43, 44, and 49-51 were rejected under 35 USC § 103(a) as being unpatentable over Ueda (U.S. Patent No. 5,787,118) in view of Coonce et al. (U.S. Patent No. 4,064,370). Applicant respectfully traverses these rejections.

Claim 1

Regarding Claim 1, in the Response to Arguments section, the Office Action dated 12/15/06 stated "it would have been obvious … to modify the memory of Ueda with the memory of Coonce et al. in order to process each data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between data paths (column 8, lines 8-22)." Applicant respectfully asserts that there is no motivation to combine Ueda with Coonce, because there is no need or desire for the device in Ueda to process each data path in sequence, or to maintain synchronization between data paths.

Applicant submits that it is not obvious, and that there is no motivation to take a buffer for one purpose and use it as a memory for an unrelated purpose. Buffer circuits are used throughout the electronics field in a variety of applications and for a variety of purposes. Many of the uses of buffer circuits are highly specialized and inapplicable to other situations. For this reason a person of ordinary skill in the art would not look to a buffer circuit used to fix one problem when trying to solve an unrelated problem in their application.

Applicant respectfully submits that combining the buffer circuits of Coonce et al. with the memory of Ueda presents such a situation. Coonce et al. uses each buffer circuit 205 as a sequentializer which temporarily delays processing of data to ensure proper timing of the data. Data received by the device of Coonce et al. may arrive approximately one-half of a time slot late due to inherent transmission delays. Col. 7, lines 26-31. Coonce et al, therefore, stores each piece of data in a buffer circuit 205 to ensure that each piece of data is processed sequentially and without gaps when released for processing. Col. 5, lines 37-67.

Ueda, in contrast, uses memory devices 43, 44 as gatekeepers which each hold a separate result from a different equalizer until one result is selected for output. The device of Ueda contains two data paths which are equalized by their respective equalizers 41, 42. Col. 20, line 33 – Col. 21, line 20. The device of Ueda can only use one of the data paths, and must provide time to decide which data path to use before the data is output. The results of each equalizer 41, 42, therefore, are held in memory devices 43, 44 while comparator 47 decides which result to select for use. The other result is discarded and not used. Col. 21, lines 1-33. Memory devices 43 and 44, therefore, cannot be used to maintain synchronization, because Ueda does not even use both data signals. Ueda, therefore, has no motivation to store the output from equalizers in a memory for the duration of a time slot as taught by Coonce et al. As a result, applicant respectfully requests that claim 1 be allowed.

Claims 2-6 depend either directly or indirectly on claim 1 and, as a result, applicant respectfully requests that claims 2-6 be allowed.

Claim 28

Regarding claim 28, the Office Action dated 05/31/06 stated that Ueda and Coonce et al. "disclose all the limitations of claim 28 (see rejections of claims 1)." Since there is no motivation or suggestion to combine Ueda and Coonce et al. according to the argument of claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 28, applicant respectfully requests that claim 28 be allowed.

Claims 29-32, 35-36 depend either directly or indirectly on claim 28 and, as a result, applicant respectfully requests that claims 28-32, 35-36 be allowed.

Claim 37

Regarding claim 37, the Office Action dated 05/31/06 stated that Ueda and Coonce et al. disclose all the limitations of claim 37. Since there is no motivation or suggestion to combine Ueda and Coonce et al. according to the argument of claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 37, applicant respectfully requests that claim 37 be allowed.

Claims 38, 39, 43, 44 depend either directly or indirectly on claim 37 and, as a result, applicant respectfully requests that claims 38, 39, 43, 44 be allowed.

Claim 49

Regarding claim 49, the Office Action dated 05/31/06 stated that Ueda and Coonce et al. disclose all the limitations of claim 49. Since there is no motivation or suggestion to combine Ueda and Coonce et al. according to the argument of claim 1, and since neither Ueda nor Coonce et al. alone disclose all the limitations of claim 49, applicant respectfully requests that claim 49 be allowed.

Claims 50-51 depend either directly or indirectly on claim 49 and, as a result, applicant respectfully requests that claims 50-51 be allowed.

Claim 9

Claims 9 and 10 have been cancelled.

Claim 21

Claims 21-26 have been cancelled.

Claim 45

Claims 45 and 48 were rejected under 35 USC § 103(a) as being unpatentable over Yaguchi (U.S. Patent No. '584) in view of Kameya (U.S. Patent No. 4,313,202). Claim 45 has been amended.

Regarding claim 45 the Office Action date 05/31/06 stated "it would have been obvious … to modify the equalizers of Yaguchi with the filtering as taught by Kameya to select of the best path based on the filters and the decoders since Kam[e]ya states the filtering can perform compromise equalization (column 5, lines 2-9, wherein equalization compensates for delay)." However, applicant respectfully asserts that neither Yaguchi, nor Kameya disclose "loading coefficients for a burst transmission into a plurality of parallel equalizers".

Claim 11

Claims 11-16 have been cancelled.

Claim 17

Claim 17 has been cancelled.

Claim 40

Claims 40 and 41 were rejected under 35 USC § 103(a) as being unpatentable over Ueda (U.S. Patent No. '118) in view of Coonce et al. (U.S. Patent No. '370) as applied to claim 37, and in further view of Zak et al. (U.S. Patent No. '926).

Regarding claim 40 and 41, the Office Action dated 05/31/06 stated that Ueda, Coonce et al., and Zak et al. disclose all the limitations of claims 40 and 41. As stated with respect to clam 37, there is no motivation or suggestion to combine Ueda and Coonce et al. Claims 40 and 41 depend directly on claim 37 and, as a result, applicant respectfully requests that claims 40 and 41 be allowed.

Claim 46

Claim 46 was rejected under 35 USC § 103(a) as being unpatentable over Yaguchi (U.S. Patent No. '584) in view of Kameya (U.S. Patent No. '202) as applied to claim 45, and in further view of Ueda (U.S. Patent No. '118). Claim 46 depends directly from claim 45 and, as a result, applicant respectfully requests that claim 46 be allowed.

Claim 47

Claim 47 was rejected under 35 USC § 103(a) as being unpatentable over Yaguchi (U.S. Patent No. '584) in view of Kameya (U.S. Patent No. '202) as applied to claim 45, and in further view of Zak et al. (U.S. Patent No. '926). Claim 47 depends directly from claim 45 and, as a result, applicant respectfully requests that claim 47 be allowed.

Allowable Subject Matter

The Examiner indicated that claim 19, 20, and 52-56 are allowable over the prior art. Applicant thanks Examiner for the indication that claims 19, 20, and 52-56 are allowable.

CONCLUSION

Applicant respectfully submits that claims 1-6, 19-20, 28-32, 35-41, and 43-59 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

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